Building the Future of Silicon: A Comprehensive IC Development Training Program

Target Audience:

- Education Government Officials
- Educators
- Prospective Students (New EE Graduates & beyond)

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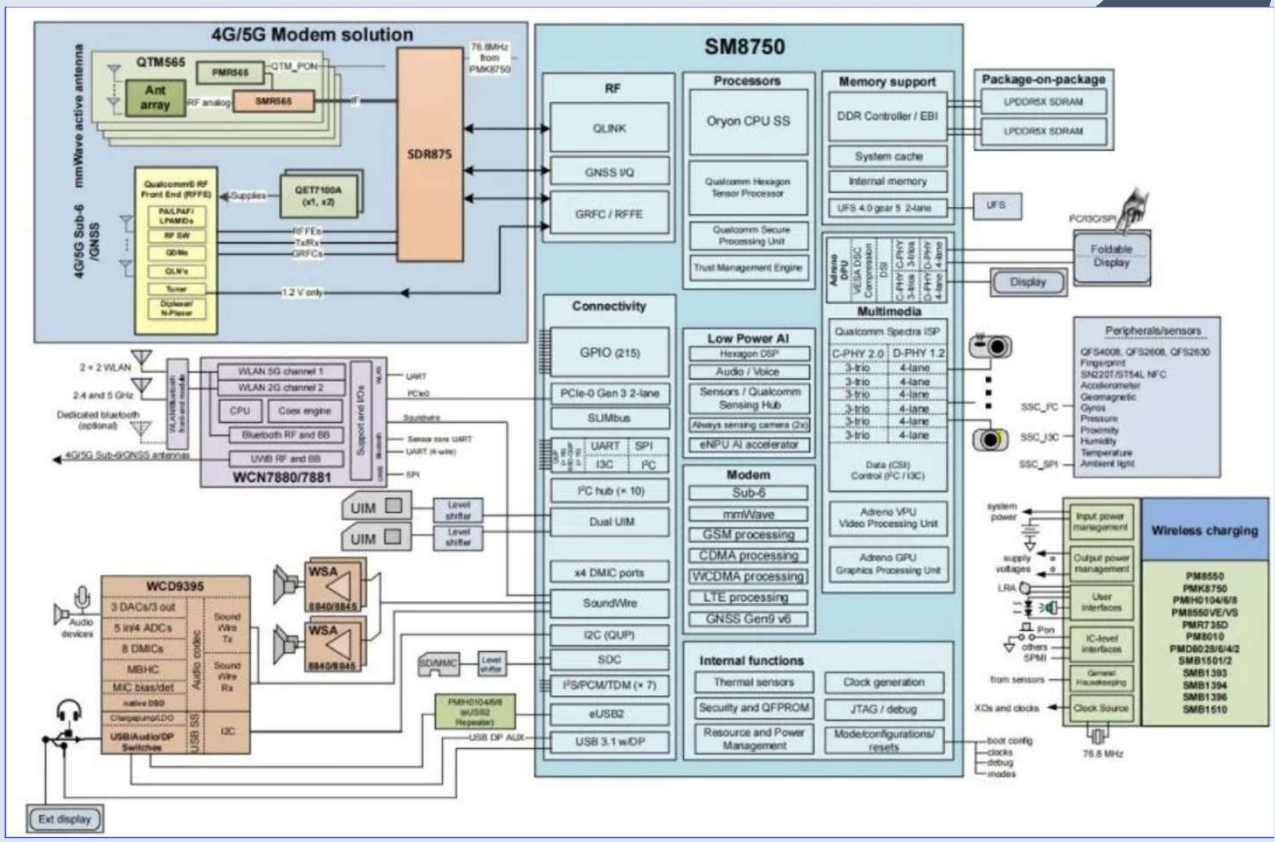
The Engine of Modern Technology: Integrated Circuits

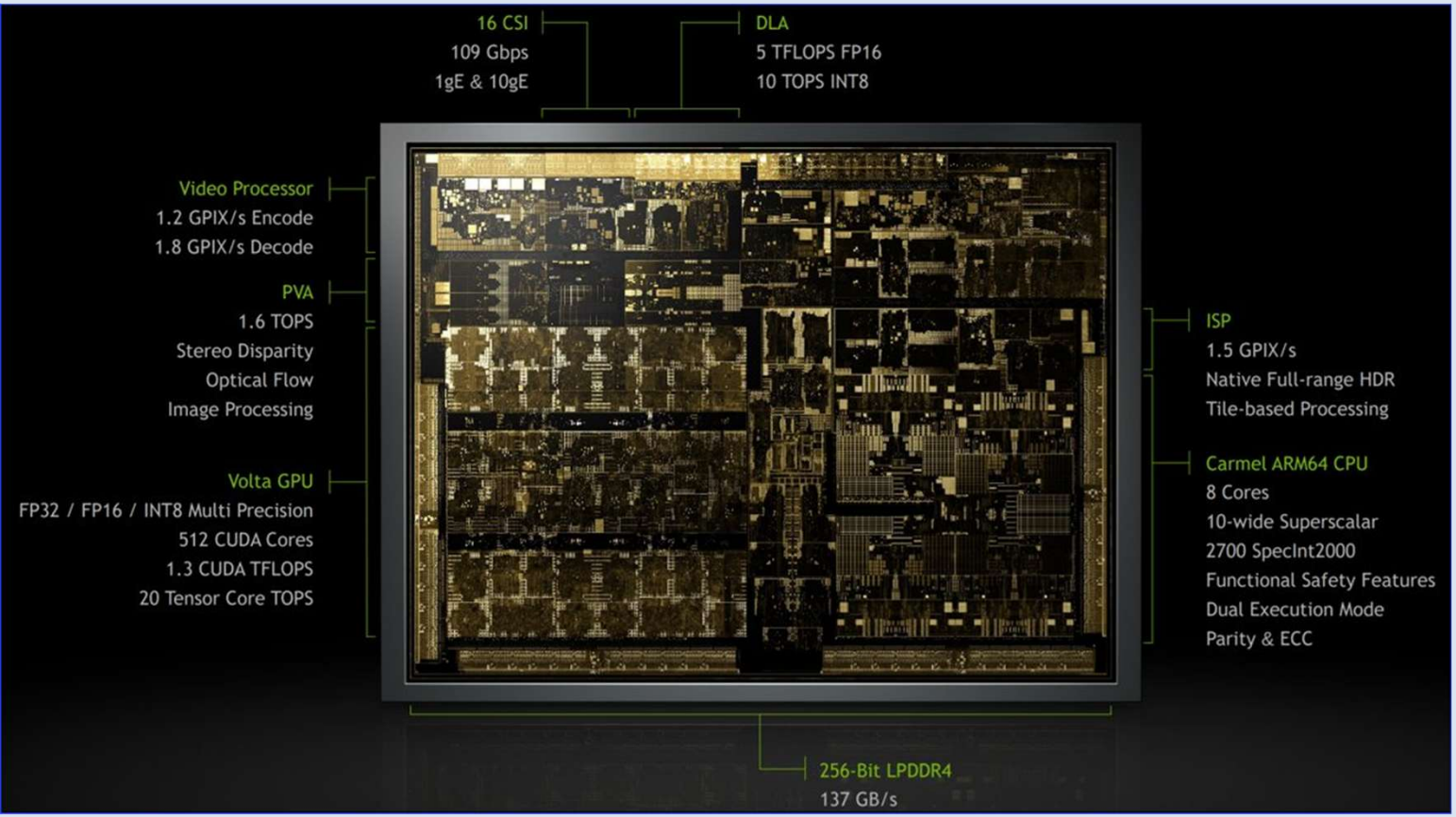
- Integrated Circuits (ICs), especially Systems-on-Chip (SOCs), are the foundation of virtually all modern technology: smartphones, AI, cloud computing, automotive systems, healthcare devices, communications.
- The semiconductor industry is a critical driver of innovation and economic growth, particularly here in Silicon Valley.
- Designing these complex chips requires highly specialized skills.
- **Purpose of this Presentation:** To introduce a comprehensive training program designed to cultivate the next generation of IC design and verification engineers.

The Challenge: Exponential Growth in SOC Complexity

- **Modern SOCs** are "universes on a chip":
  - § **Scale**: Billions of transistors, integrating 10s to 100s of millions of logic gates.
  - § **Integration**: Combining diverse, complex IP blocks (CPUs, GPUs, AI/ML accelerators, high-speed interfaces, analog components).
  - § **Concurrency**: Numerous blocks operating and interacting simultaneously over complex interconnects (NoCs, buses).
- **Result:** Designing and verifying these systems is incredibly challenging, pushing the limits of current tools and methodologies.



Example: Qualcomm SOC - Snapdragon 8 Gen 4
https://www.gizmochina.com/2024/10/06/big-snapdragon-8-gen-4



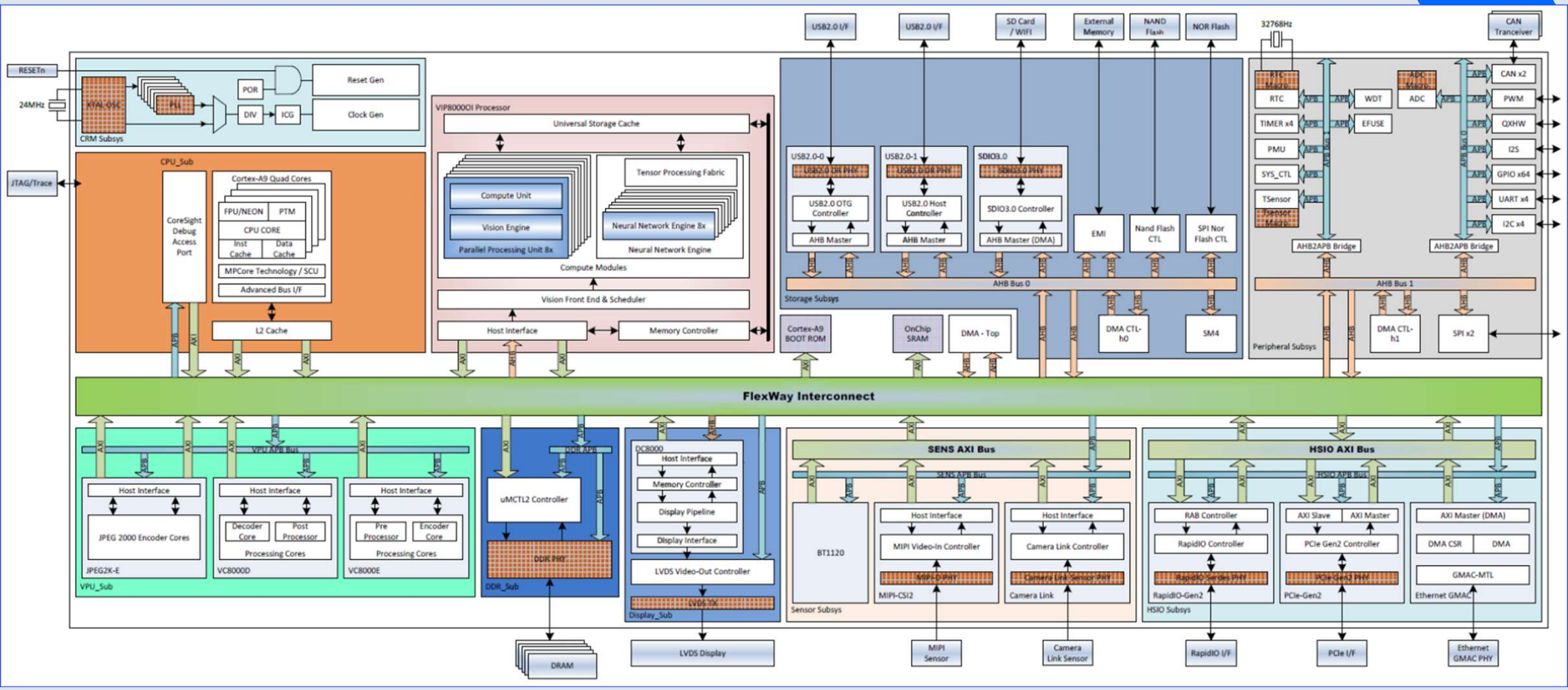
Example:

NVIDIA Xavier AI SOC (Circa 2018)
Transistors: 9 billion transistors
Tech Node: TSMC 12nm process
Die Size: 350 mm2.
Architecture:
- 8x ARM64 CPU
- 512 CUDA Cores
- 20 Tensor Cores
- 16 GB 256-bit LPDDR4

TDP: 30W

Investment:
- 2K+ Engineers,
- 4 years,
- $42B R&D

In 2025, SOC is even more grand.



Example: HISAOR-03A AI SOC for embedded AI applications

https://ocetechnology.com/hisaor-rad-tolerant-ai-soc/

Industry Pressures & The Skills Gap

- **Time-to-Market:** Intense competition demands shorter design cycles.
- **Cost of Errors:** Silicon re-spins (fixing bugs after manufacturing) cost millions and cause major delays. "First-Time Correct Silicon" is the goal.
- **"Shift Left":** Industry focus on finding bugs earlier in the design cycle (pre-silicon) through advanced verification and simulation.
- **The Skills Gap:**
  - University programs provide excellent theoretical foundations,
  - but there's often a gap between
    - Academic knowledge and
    - The specific, practical skills, tools (e.g., SystemVerilog, popular EDA tools), and methodologies (e.g., UVM awareness) required for immediate productivity in industry roles.
- **Our program aims to bridge this gap.**

Our Vision: Industry-Ready IC Engineers

- **Mission**: To provide intensive, practical training that transforms recent Electrical Engineering graduates into proficient IC Design and Verification Engineers equipped with industry-standard skills.
- **Focus**:
  - **Practical Application:** Emphasis on hands-on labs and real-world design/verification scenarios.
  - **Modern Standards:** Utilizing SystemVerilog (the industry standard HDL/HVL) and concepts from leading methodologies (UVM foundation).
  - **Industry Tools:** Training based on widely-used EDA tool flows.
- **Comprehensive Scope**: Covering the flow from design specification concepts through to physical implementation awareness.

Program Philosophy: Holistic Development

- Developing a proficient IC engineer requires more than just technical depth; it needs context, foundational reinforcement, essential practical tools, professional skills, and applied project experience.
- Our program is structured to provide this holistic development:
  - § **Context**: Understanding the "Big Picture" of SOC teams and roles.
  - § **Foundation**: Reviewing and connecting core EE principles to IC design.
  - § **Toolbox**: Equipping students with essential development environment skills.
  - § **Core Technical Skills**: In-depth training in SystemVerilog, Synthesis, and Physical Design.
  - § **Advanced Topics**: Modules covering critical areas like DFT, Low Power, Timing, and advanced verification techniques.
  - § **Professionalism & Context**: Integrating soft skills, process awareness, and project context.
  - § **Application**: Capstone projects to integrate and demonstrate acquired skills.

Program Structure - Stage 1: Foundation & Preparation

- Ensuring readiness and setting the context:
  - **Knowledge Assessments**: Tailoring the program based on individual background checks.
  - **The "Big Picture" Introduction**: Understanding SOC complexity, team structures, roles (System/SOC/Domain Arch, FE, VE, BE, Test, Validation), and the critical importance of verification.
  - **Foundational Concepts Review**: Connecting core EE knowledge (Signals, CMOS, Gates, Logic Design) to HDL concepts and modeling rationale (e.g., 4-state logic).
  - **Essential Toolbox:** Practical skills in Unix environments, code editors (VS Code), basic IC design IDEs, scripting (Python), source code management (e.g., Git), and essential C/C++ for embedded context.
  - **Soft Skills & Mindset**: Developing integrity, effective communication, customer focus, collaboration, and documentation habits necessary for team success.

Program Structure - Stage 2:
Core Technical Skills - SystemVerilog

- Mastering the industry-standard language for design and verification:
  - **SV Fundamentals & Modeling (C1, C2):** Core syntax, data types, procedures, simulation basics, standard cell/macro modeling, specify blocks.
  - **SV for RTL Design (C3):** Writing efficient, synthesizable SystemVerilog, combinational/sequential logic, FSMs, hierarchy, parameterization, interfaces, DFT/Power awareness for designers. (Target: FE Design Engineers)
  - **SV Verification Foundation (C4):** OOP for verification, building modern testbench structures (Interfaces, VIFs, Clocking Blocks), IPC, randomization, coverage concepts, assertions (SVA). (Foundation for Verification Engineers)
  - **SV Test Dev & UVM Focus (C5):** Applying UVM concepts, base classes, sequences for stimulus generation, scoreboards, RAL introduction, test execution & control. (Core skills for Verification Engineers)
  - **SV for Mixed-Signal Verification (C6):** Verilog-AMS concepts, behavioral modeling, connecting digital testbenches to analog/mixed-signal blocks. (Specialized Verification Engineers)

Program Structure - Stage 3:
Core Technical Skills - Implementation Flow

- Implementation Flow - Understanding how RTL becomes silicon:
  - **Logic Synthesis Course (Introductory):**
    - § **Focus**: RTL-to-Gates translation, optimization.
    - § **Skills**: Synthesis flow, tool usage (e.g., Design Compiler context), writing synthesis-friendly RTL, Static Timing Analysis (STA) basics, constraining the design (SDC), meeting Power, Performance, Area (PPA) goals.
    - § **Relevance**: Critical for FE Designers, context for BE/VE.
  - **Physical Design Course (Introductory):**
    - § **Focus**: Gate-level Netlist-to-Layout (GDSII).
    - § **Skills**: PD flow (Floorplanning, Place, CTS, Route), Timing/Power/Signal Integrity closure with PD tools, physical verification (DRC/LVS).
    - § **Relevance**: Critical for BE (Physical) Designers, context for others.

Program Structure - Stage 4: Industry Context & Professionalism

- Understanding the ecosystem and professional practices:
  - **Design Flow Interfaces**: Handoffs and data exchange between
    - Architecture <-> Front-End,
    - Front-End <-> Back-End,
    - Back-End <-> Manufacturing.
  - **Manufacturing Test Basics**: Introduction to ATE, yield concepts, failure analysis interface.
  - **Project Management Context**:
    - Understanding SOWs,
    - planning/tracking, team roles (Engineers, Project Manager, Program Manager),
    - communication needs,
    - considerations for engineers working in project teams (including outsourcing context).

- **Goal**: Prepare engineers to work effectively within large organizations and complex projects.

Program Structure - Stage 5: Applied Capstone Projects

- **Purpose:** To synthesize knowledge and apply skills learned across the entire program to realistic, industry-relevant projects. This stage bridges focused learning with practical execution.
- **Project Examples:** Students engage in substantial projects such as:
  - § **Design & Verification of Standard Peripherals**:
    Implementing and verifying blocks like SPI controllers, I2C interfaces, or UARTs.
  - § **Adoption & Verification of Custom Hardware Acceleration Modules**:
    Contributing to open-source hardware design IP's.
  - § **Design & Verification of AMBA Bus Components**:
    Creating and testing behavioral models for bus infrastructure like APB Slaves/Masters, AXI Lite/Full Slaves/Masters, or basic AXI Interconnects/Switches.
  - § **Verification of Open-Source IPs**:
    Applying learned verification techniques (UVM testbenches, coverage, assertions) to existing complex, open-source hardware designs such as OpenTitan or LowRISC/IBEX
- **Skills Applied:** Integrates RTL design, UVM testbench development, synthesis awareness, coverage-driven verification closure, debug strategies, potential scripting, and project planning/documentation.
- **Outcome:** A significant portfolio piece demonstrating integrated, practical IC development capabilities highly valued by employers.

Program Structure - Stage 6: Specialized Topics (Advanced, On Demand)

- Providing depth in critical, modern SOC development areas, based on request:
  - **Advanced Simulation & Embedded Verification**: RTL/Gate/Mixed-level simulation flows, debugging complex systems, testbenches for embedded CPUs (e.g., ARM), co-verifying SystemVerilog and C-based tests via DPI.
  - **FPGA Emulation & Validation**: Using FPGAs for pre-silicon system validation and accelerated verification.
  - **Timing & Signal Integrity Closure**: In-depth Static Timing Analysis (STA), cross-talk, noise analysis, and timing closure techniques.
  - **Low Power Design & Verification (In-depth):** UPF-based flows, power estimation, low-power techniques verification, power domain interactions.
  - **Design For Test (DFT) (In-depth):** Scan insertion, ATPG, BIST (Logic & Memory), compression, JTAG/SWD, SOC-level test strategies.
  - **Physical Design (In-depth):** PD flow (Floorplanning, Place, CTS, Route), Timing/Power/Signal Integrity closure with PD tools, physical verification (DRC/LVS).

Goal: Equip engineers for specialized roles and complex challenges.

Key Program Features & Benefits

- **Industry-Standard Focus:** SystemVerilog, UVM concepts, popular tool flow context, relevant automation (Register/SOC Assembly concepts).
- **Practical & Hands-On:** Extensive labs reinforce theory and build crucial EDA tool proficiency.
- **Capstone Project:** Culminating project demonstrates integrated skills on industry-relevant tasks, providing valuable portfolio evidence.
- **Holistic Development:** Integrates technical skills with essential soft skills and industry awareness.
- **Flexible & Tailored:** Initial assessment helps guide individual learning paths.
- **Directly Addresses Skills Gap:** Produces engineers ready for complex SOC design and verification roles.
- **Truly Comprehensive:** Covers foundational refresh, toolbox skills, core SV/Synth/PD, advanced topics (DFT, Power, Timing, Embedded V&V), and professional context.

Target Roles & Career Opportunities

- This program provides skills sought after by leading semiconductor companies, IP providers, and system houses worldwide, particularly in innovation hubs.
- Addresses the ongoing critical shortage of skilled IC development talent.
- **Capstone projects** provide graduates with demonstrable experience directly applicable to these roles.
- Prepares graduates for high-demand roles in the semiconductor industry:
  - § **Core**: RTL Design Engineer, Design Verification Engineer, Physical Design Engineer, Synthesis Engineer.
  - § **Specialized**: DFT Engineer, Low Power Engineer, STA Engineer, Mixed-Signal Verification Engineer, Emulation Engineer, Verification Methodology Engineer.

The Skills Gap Challenge: A Specific Context

Specific challenges exist in bridging the gap between university education and industry requirements, particularly in developing tech ecosystems like Vietnam.

- **Industry Expectations:** Global companies seek engineers who meet international qualification norms (deep technical skills, practical tool experience) and integrate smoothly into established work cultures.
- **University Output:** Graduates from excellent universities may have strong theoretical foundations but often lack the specific, in-depth training on industry-standard tools (e.g., SystemVerilog, UVM), advanced methodologies, and practical project experience needed for immediate contribution.
- **Language/Culture:** While English education is common, achieving the high level of nuanced technical communication (verbal and written) required in global teams can be a hurdle.
- **Outsourcing Needs:** Companies needing temporary/outsourced engineers require resources with prior industry experience who are immediately productive. They typically do not budget for extensive on-the-job training for short-term roles.

Addressing the Gap: Past Approaches & Our Solution

- **Past/Present Approaches:**
  - Some large companies, e.g. Intel, have recognized this, occasionally partnering with international universities (e.g., US institutions) for specialized programs.
  - Selected students might attend these programs abroad, receiving certificates upon completion.
  - Companies may then hire primarily from this specific pipeline.
  - **Constraints**: These solutions are often very expensive (tuition, travel, living costs), limiting the candidate pool significantly and not scaling to meet broad industry demand.
- **Our Proposed Solution (This Training Program):**
  - We aim to provide a practical, accessible, and high-quality solution to directly address the skills gap.
  - **Bridging the Gap:** By offering this comprehensive program **locally**, focusing on:
    - **Industry-Relevant Curriculum:** Dives into SystemVerilog HDL (Design/Verification/UVM), Synthesis, Physical Design concepts.
    - **Practical Tooling:** Hands-on labs using industry-standard EDA tool flows.
    - **Professional Skills:** Integrating soft skills, communication, teamwork, and project awareness.
    - **Applied Experience:** Culminating in **capstone projects** demonstrating integrated skills.
  - **Our Aspiration:** We bring specific industry experience and goodwill to significantly reduce the skills gap and produce proficient, employable engineers.

Future Outlook: AI & Essential Engineering Skills

- Technology is rapidly changing, with **AI** poised to automate many tasks across various sectors.
- **Bill Gates' Insight:** He says "AI will replace humans for most things" in 20 years, including manufacturing and professional jobs. He specifically highlighted that only three professions would survive the AI revolution: **biologists**, **energy experts**, and **coders**. Gates indicated that these fields are too complex to be fully automated using AI, and that they still need human intervention.
- **Relevance to IC Development:**
  - The fundamental task of understanding specifications, designing complex architectures, creating intricate verification strategies, debugging system-level interactions, and applying deep engineering judgment remains highly complex.
  - The skills taught in this program – system thinking, complex digital/mixed-signal design, advanced verification techniques, sophisticated "**coding**" (HDLs, HVLs, scripts), and problem-solving – align directly with the type of complex engineering expertise expected to be essential and less susceptible to full automation by AI.
- **Conclusion**: Investing in these deep engineering skills is investing in a relevant and resilient future career path.

Conclusion: Developing Project-Ready IC Talent

- Modern SOC development demands a high level of specialized skill, efficient teamwork, and practical application ability.
- This comprehensive training program provides the necessary technical depth, foundational context, tool proficiency, professional awareness, and culminates in applied capstone projects.
- Our graduates will be equipped not just with knowledge, but with demonstrated experience to tackle the challenges of IC design and verification and contribute significantly to the semiconductor industry.
- We aspire to help build the next generation of silicon innovators.

- **Thank You & Q&A**